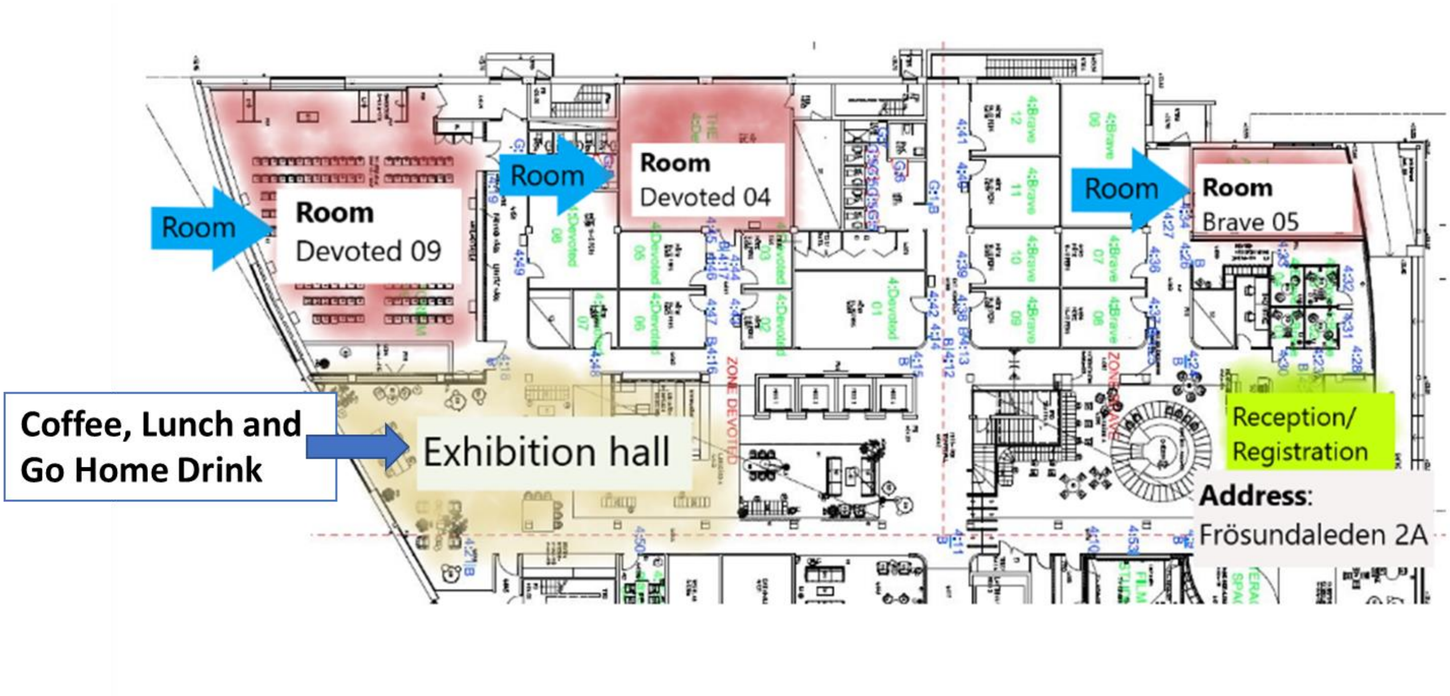
Time	Program		
08:30	**FPGAworld 2023** Registration: Stockholm, Sep 12th, AFRY, Frösundaleden 2A, 169 70 Solna, SWEDEN		
Sponsors 2023			
09:00	**Conference Opening** Henrik Rosendahl, AFRY and Lennart Lindh, FPGAworld **Room:** Devoted 09		
09:15-10:00	**Keynote** **Title: Key Factors for Success in Today's and Tomorrow's Markets** **Keynote speaker:** Mark Frost, Intel's Programmable Solutions Group (previously Altera), England **Abstract:** This presentation will explore the fundamental components necessary for FPGA suppliers to succeed, including supply chain management, product leadership, and an up-to-date developer experience. Analysis of the current supply chain landscape and its challenges, as well as strategic investments for product leadership and competitiveness, will be discussed. The importance of having the correct knowledge and skills, EDA tools, SoCs, and IP from generation to generation for FPGA developers will be examined. Furthermore, an overview of the options, standards, and flows available to FPGA vendors and applications of FPGA technology in different parts of the world will be provided, finishing with a prediction of the future of FPGA technology. **Session Chair:** Lennart Lindh, FPGAworld/AGSTU		
10:00-10:30	**Coffee Break & Exhibition**		
10:30-12:00 3*30 min	**Track** **Session Chair:** Tommy Klevin, AFRY **Room:** Devoted 09	**Track** **Session Chair:** Magnus Karlsson, Innowicom **Room:** Devoted 04	**Track** **Session Chair:** Tobias Karlsson, AFRY **Room:** Brave 05
	Title: Microchip FPGAs: Ensuring: security, reliability, safety, and time to market, through AMP, OSs and RTOS **Presenter**: Hugh Breslin, Microchip Technology GmbH, Germany More_information **Title:** FPGA and board design patterns to aid (MTBF and) SEU-aware loss-of-function quantitative estimates. **Presenter:** Cristian Ciressan, Enclustra GmbH, Switzerland More_information **Title:** Demonstration Setup for HashCache **Presenter:** Philipp Keydel, Synogate, Germany	**Title:** Prototyping and Verifying Wireless Systems on FPGA **Presenter:** Daniel Aronsson, MathWorks, USA **Title:** European Cyber Resilience Act and its impact on IEC62243 and embedded system security. **Presenter:** Matt Holdsworth, Senior Applications Engineering Lattice, North Europe. **Title:** Introduction to Accelerated PCBA Testing and Programming. **Presenter:** Tommaso De Vivo, Vice President Business Development EMEA – XJTAG Presenters, UK	**Title:** Review of Forth Soft-Core Processors **Presenter:** Christopher Lozinski, Silesian Polytechnical University, Poland More_information **Title:** Why are RISC-V® and TinyML a good path to scalable low power AI deployment at the Edge? **Presenter:** Joachim Mueller, FAE Manager Europe, Efinix Inc More_information **Title:** IP replication and partial reconfiguration using an FPGA with 2D NoC **Presenter:** Simon Longcroft, Achronix, USA More information
12:00-13:00	**Lunch Break & Exhibition SPONSOR**		

	VUnit Track **Session Chair:** Lars Asplund, Synective labs **Room:** Devoted 09	**Track** **Session Chair:** Magnus Karlsson, Innowicom **Room:** Devoted 04	**Track** **Session Chair:** David Källberg, IAR **Room:** Brave 05
13:00- 14:30 3*30 min	**Title:** VUnit integration into existing code base and leveraging verification components for better testbenches **Presenter:** Sebastian Hellgren, CodeCache Linköping AB, Sweden More_information **Title:** Enhancing MathLib Development through VUnit-Powered Unit Testing **Presenter:** Kunal Panchal och Balaji Chirumamilla, King's College London **Title:** Abusing the VUnit test runner for FPGA build automation **Presenter:** Ludvig Vidlid, Truestream AB, Sweden More information	**Title:** Cross-vendor model-based RTL design with the OSS Whiznium developer tools **Presenter:** Alexander Wirthmüller, MPSI Technologies GmbH, Germany More information **Title:** Creating 4k/8k video applications with Intel Agilex FPGAs **Presenter:** Alexey Lopich, Arrow/Intel, USA **Title:** The Invincible TCP Core: Servicing all Devices on the Internet from one FPGA **Presenters:** Philipp Keydel, Synogate, Germany	**Title:** New Intel FPGAs for mid-range applications **Presenter:** Mark Frost, Arrow/Intel, USA **Title:** Lattice Avant, a new level of low power FPGA innovation for mid-range applications. **Presenter:** Matt Holdsworth, Senior Applications Engineering Lattice, North Europe. **Title:** Low Power and Performance for Edge Applications - and beyond **Presenter:** Joachim Mueller, FAE Manager Europe, Efinix, USA More_information
14:30-15:00	**Coffee Break & Exhibition**		
	Microchip Track **Session Chair:** Kim Petersen, HDC **Room:** Devoted 09	**Demo UVVM Track** **Session Chair:** Espen Tallakesen, TechSeed EmLogic **Room:** Devoted 04	**Track** **Session Chair:** David Källberg, IAR **Room:** Brave 05
15:00- 15:59 2*30 min	**Title**: Functional Safety in FPGA Designs **Presenter**: Martin Kellermann, Microchip Technology GmbH, Munich **Title**: Introduction to Vector Processing and Neural Network Acceleration on Microchip FPGAs **Presenter**: Brian Colgan, Microchip Technology GmbH, Dublin	**Title:** Demo: Making a simple but structured VHDL testbench – for beginners **Presenter:** Espen Tallakesen, EmLogic, Norway **Time:** 1 hour More information	**Title:** Introduction to Accelerated PCBA Testing and Programming. **Presenter:** Tommaso De Vivo, Vice President Business Development EMEA – XJTAG Presenters, UK **Title:** Radiation-tolerant design and verification concepts **Presenter:** Dr. Reuven Dobkin, CTO of vSync Circuits
16:00- 16:45	**Keynote** **Title: RISC-V: Paving the Path Together to a Safe, Secure and Reliable Future** **Keynote speaker:** Martin Kellermann, Microchip Technology GmbH, Munich **Abstract:** This keynote will explore the potential of RISC-V, an open-source instruction set that allows companies of all sizes to gain the benefits of independence and innovation. It will discuss its potential to shape the future of computing and how companies can use it to create applications such as High-Performance Spaceflight Computing (HPSC) processors. It will also highlight companies that are already a part of this revolution and the ecosystems that enable easy adoption and scalability for a safe and secure future. Together, we can make great strides with RISC-V. **Session Chair:** Lennart Lindh, FPGAworld/AGSTU		
16:45 -	**Go Home Drink in the Exhibition Hall**		
Sponsors, exhibitors and/or presenters Copenhagen and Stockholm	DTU, Technical University of Denmark AFRY, Sweden Aktuel Elektronik, Denmark AGSTU FPGA Education, Sweden XJTAG, UK Microchip, UK Intel PSG, USA Efinix, USA Truestream AB, Sweden MathWorks, USA	Achronix, USA Lattice Semiconductor, USA Synective Labs, Sweden SynoGate, Germany Emlogic, Norway Enclustra GmbH, Switzerland Avnet Silica, Denmark BitSim NOW, Sweden Trenz Electronic GmbH, Germany MathWorks, USA	CodeCache Linköping AB, Sweden MPSI Technologies GmbH, Germany Arrow, Europe Avnet Silica, Sweden XPERI, USA VSYNC, Israel King's College London, UK Motion Control, Sweden FPGAworld, Sweden

Welcome to FPGAworld Conference 2024, 10 September Stockholm, and 12 September in Copenhagen 2024

More information



Keynote speaker: Mark Frost, Intel's Programmable Solutions Group (previously Altera), England
Title: Key Factors for Success in Today's and Tomorrow's Markets
Abstract: This presentation will explore the key areas that FPGA suppliers must consider in order to succeed: industry-leading supply chain management, product leadership, and an up-to-date developer experience. We will examine the current supply chain landscape, which is facing an unprecedented imbalance in demand and supply, leading to long lead times and product allocations. We will also discuss the need for FPGA companies to make strategic investments to achieve product leadership and remain competitive. Furthermore, we will look at the importance of having up-to-date knowledge and skills, fast and appropriate EDA tools, the right SoCs, and the right RTL, SW, and hardware IP from generation to generation for FPGA developers to be productive. The presentation will then provide an overview of the different options available to FPGA vendors, preferred standards, and flows. Finally, we will look at how FPGA technology is being used in different parts of the world and provide a prediction of its future.
CV: Mark is the FPGA Security and 5G Technical Marketing Manager within Intel's Programmable Solutions Group (previously Altera). Within this role Mark liaises between customers, sales and engineering teams worldwide for security and 5G communication topics, and works to create market awareness of Intel's portfolio. During his 11 years with Intel he has held roles in both marketing and as a field application engineer covering programmable technology. Prior to Intel, Mark had worked for over 15 years in a variety of engineering roles, spanning telecommunications through to designing instruments for ESA satellites. Mark has a BEng in Electrical Engineering from the University of Plymouth.

Keynote Speaker Stockholm
Title: RISC-V: Paving the Path Together to a Safe, Secure and Reliable Future
Keynote speaker: Martin Kellermann, Microchip Technology GmbH, Munich
Abstract: RISC-V is an open-source instruction set that has created opportunities for companies of all sizes to innovate and make decisions independently. It is predicted to shape the future of computing for the next 50 years by providing a processor architecture that allows for more processing with a smaller carbon footprint, more features with less development resources, and new ways to combat threats with existing technologies.

Companies are already utilizing RISC-V to develop applications such as High-Performance Spaceflight Computing (HPSC) processors. This keynote will explore how companies can benefit from this independence and how the ecosystems can enable easy adoption and scalability. It will also highlight companies that are already a part of this revolution and discuss how they can help create a safe and secure future. Through RISC-V, companies can reach their goals and protect their future. Together, we can move mountains.
CV: Martin Kellermann is an experienced FPGA and SoC engineer with a diploma in Electrical Engineering from the Landshut University of Applied Sciences. He has expertise in high-speed serial data transmission, signal integrity, and hardware debugging, successfully delivering projects in the industrial, automotive, and data-center domains. As Marketing Manager at Microchip Technology GmbH, Munich, he works with the European Sales and Field Application team to showcase the strengths of their FPGAs and SoCs.

Presentations

Radiation-tolerant design and verification concepts
Presenter: Dr. Reuven Dobkin, CTO of vSync Circuits
Abstract:
FPGA designs for space must operate under harsh radiation conditions. The radiation can cause multiple types of hard (ubrecoverable) and soft (recoverable) functional failures. During this lecture, we will review a few RTL design development guidelines for space applications that are also applicable for non-space safety-critical applications. We will discuss how space quality assurance can be achieved using static tool-based verification process.

Title: Enhancing MathLib Development through VUnit-Powered Unit Testing
Presenter: Kunal Panchal och Balaji Chirumamilla, King’s College London (KCL)
Autors; Srinivasan Venkataramanan, AsFigo Technologies, UK, Anirduh Pradyumnan Srinivasan, Undergraduate at King’s College London (KCL), Kunal Panchal and Balaji Chirumamilla
Abstract:
MathLib is an open-source library developed to support complex mathematical functions in digital designs – to provide compatible features to MATLAB™. To make MathLib production ready, we deployed systematic testing methodologies in ensuring the accuracy and robustness of these functions. We show test suites & test cases targeting MathLib's individual functions, showcasing how Vunit's ease-of-use streamlines the testing process. Here are some of the benefits of using VUnit + SystemVerilog to unit test MathLib:

- Early testing: VUnit can be used to start unit testing MathLib early in the development process. This can help to catch bugs early and prevent them from becoming major problems later.
- Automated testing: VUnit can automatically run the test suites and check individual MathLib functions.
- Increased confidence: Unit testing with VUnit can help to increase confidence in the correctness of MathLib.

Title: Low Power and Performance for Edge Applications - and beyond
Presenter: Joachim Mueller, FAE Manager Europe, Efinix, USA
Abstract:
Titanium FPGA family is the second-generation FPGA introduced by Efinix Inc, Cupertino (California). While the first generation is used in many products already, Titanium consistently continues the path of solving special requirements not only but especially for edge applications. Among those requirements are size, power consumption, support for certain functions. The presentation takes a tour through Titanium general features and the specific ingredients as of today. To assess why Titanium is a good choice for the edge and beyond the presentation will conclude with an insight into power consumption, and an up-to-date snapshot of upcoming expansions in terms of new features and new devices.

Title: The Invincible TCP Core: Servicing all Devices on the Internet from one FPGA
Presenters: Philipp Keydel, Synogate, Germany
Abstract:
The future of high-speed networking: our hostless TCP core with groundbreaking speed and capacity. It harnesses Synogate HashCache, a CAM-like state table with built-in age-based session management. Fully hardware-implemented, it is invulnerable to any kind of software attacks. With hundreds of millions of inserts per second, it is DDoS-resilient. DRAM allows holding billions of concurrent connections, making it suitable for internet exposure. Reimagine the limits of your networking devices.

Title: Lattice Avant, a new level of low power FPGA innovation for mid-range applications.
Presenter: Matt Holdsworth, Senior Applications Engineering Lattice, North Europe.
Abstract:
Lattice Avant is a new FPGA platform purpose-built to bring the Lattice's power efficient architecture, small size, and performance leadership to mid-range FPGAs. Explore Avant's features, that offer best-in-class power efficiency, advanced connectivity, and optimized compute, all in a small footprint. Find out how the design choices for Avant architecture resulted in power and performance optimizations. Learn about the Avant-E family and portfolio of development tools to get you started on developing with Avant.

Title: European Cyber Resilience Act and its impact on IEC62243 and embedded system security.
Presenter: Matt Holdsworth, Senior Applications Engineering Lattice, North Europe.
Abstract:
Many nation states and collectives of them are now embracing the concepts of Cyber Resilience. The most recent example is the European Commission's Cyber Resilience Act. Prior to this, the United States National Institutes of Standards and Technology (NIST) had published a seminal guideline with the NIST Special Publication 800-193, entitled Platform Firmware Resilience which is not a de-facto standard applied to all major Hyperscaler Servers. This summer the Trusted Computing Group (TCG) released their Cyber Resilient Module and Building Block Requirements. In this paper we will highlight how using strong Root of Trust (RoT) FPGA technologies can help implement best practices with regards to CyberResilient Systems to meet the coming compliance implementations from the EC Cyber Resilience Act, as well as NIST SP 800-193 Platform Firmware Resilience Guidelines and the TCG Cyber Resilient Module and Building Block Requirements. Topics covered will include the fundamental Protect-Detect-Recover cycle of Cyber Resilient Systems and how best to implement such a cycle using RoT FPGA technologies which are well suited for demands of a real-time cyber resilient system. Additionally, the security paradigm change concepts that Cyber Resilience is ushering will be detailed. Such as the required mindset change from avoiding a cyber-attack to accepting the high probability of attack and how to best operate through it with minimal to no damage (a fundamental of cyber resilience).

Title: New Intel FPGAs for mid-range applications
Presenter: Mark Frost, Arrow/Intel, USA
Abstract:
The wait is finally over! Intel PSG has a new roadmap for mid-range FPGAs, ideally suited to video, vision and broadcast applications. Attend this short session to gain an overview of this brand-new mid-range FPGA product, an addition to the cutting-edge Agilex family.

Title: Creating 4k/8k video applications with Intel Agilex FPGAs
Presenter: Alexey Lopich, Arrow/Intel, USA
Abstract:
4k and 8k video applications can be technically demanding to implement within FPGAs, often with clock frequencies exceeding 600MHz. Attend this session to find out why FPGAs can be used in these applications, along with some implementation guidelines for Intel Agilex FPGAs.

Title: Introduction to Accelerated PCBA Testing and Programming.

Presenter: Tommaso De Vivo, Vice President Business Development EMEA – XJTAG Presenters, UK
Abstract:
Did you know a JTAG connection allows you to test a board using boundary scan via its FPGA? It overcomes the lack of physical access caused by BGAs and high-density PCBs by using FPGA pins as virtual test probes. They can be read and controlled without configuring the device, and many engineers in all industrial sectors now use boundary scan for board bring-up and test.
This talk introduces the technology and shows how XJTAG provides an easy-to-use method to test and program PCBAs.

Title: Review of Forth Soft-Core Processors
Presenter: Christopher Lozinski, Silesian Polytechnical University, Poland
Abstract:
Forth on a stack machine in an alternative to using C on a soft core register machine.
Forth is a reverse polish notation (RPN) programming language which runs on many platforms. A Forth core is a very small stack machine. Forth includes an interpreter, which makes it great for debugging hardware. The Propeller Parallax even includes a Forth interpreter in ROM, for just this reason. A Forth program requires very little memory, making it perfect for FPGAs. The Core-1 Forth interpreter itself consumes no memory, it is entirely implemented in circuitry.
Historically there have been many Forth cpus. The low power RTX2010 in Philae recently landed on a comet. More recently there are 15 known soft-core Forth processors. The J1a is particularly small, it just copies bits from a camera to tcp/ip. The EP32/24/16 has gorgeous documentation. The MicroCore is very mature and has hardware support for Cooperative Sequential Processes (CSP). The Core-1 is the new kid on the block, written in System Verilog.
Forth will be compared to using C on a soft core register machine.
CV:
Christopher Lozinski is an MIT graduate, serial entrepreneur, dual US-EU citizen, long time Python developer and polyglot. Instead of seeking Venture Capital, he moved from Silicon Valley to Katowice Poland. Recently he returned to graduate school in digital electronics, built a frequency and duty cycle meter, and was approved to build a Forth CPU for his master's project.
Place or places: Stockholm

Title: Microchip FPGAs: Ensuring: security, reliability, safety, and time to market, through AMP, OSs and RTOS
Presenter: Hugh Breslin, Microchip Technology GmbH, Germany
Abstract:
Designers want to create the safest, most secure and most reliable systems on the market, whilst also wanting to get to market as fast as possible. But, how do you balance these efforts? In this presentation, we will explore how Microchip enables and empowers designers to meet their requirements for both their applications. We will discuss how the proper design can help customers get to market with the knowledge that safety, security and reliability is at the forefront of what they've delivered. We will also explore the design methodologies, software and hardware implementations, and architecture required to meet these goals.

Title: FPGA and board design patterns to aid (MTBF and) SEU-aware loss-of-function quantitative estimates.
Presenter: Cristian Ciressan, Enclustra GmbH, Switzerland
Abstract:
For Safety-Critical applications, trying to estimate the loss-of-function (LoF) probability during mission time, when using COTS boards, is a creative process to say the least.
Certain assumptions are made, followed by an often ad-hoc analysis to eventually get the desired quantitative figure(s). Whether the process followed, and the results generated are accepted or not, ultimately depends on a certification authority.

We will talk about (1) a proposed formalism to address the task of (MTBF and) SEU-aware LoF estimation, (2) how this formalism is translated to certain FPGA and board design patterns and (3) provide examples of how this is applied in a few practical situations.

Title: Demonstration Setup for HashCache
Presenter: Philipp Keydel, Synogate, Germany
Abstract:
Due to the ever-growing need for fast communication, demands on middleboxes such as firewalls, VPN gateways, and DPI systems are continuously rising. To cope with hundreds of millions of packets per second (MPPS) in a single device, FPGAs are often used as dedicated network traffic processors due to their ability for massively parallel and low-latency processing. Many times, FPGAs have been used for stateless packet processing tasks (in which packets are processed in isolation), such as packet classification and forwarding. Still, for a wide variety of use cases, stateless packet processing is not sufficient, as packets must be considered in the context of connections or flows. Applications for which stateful packet processing is of paramount importance are firewalls, DPI systems, and DDoS mitigation systems. However, existing approaches on FPGA-based stateful packet processing are either slow, cannot deal with high update rates, and/or have to fall back on expensive components such as off-chip TCAMs.
To solve this problem, we developed HashCache, a high-performance stateful packet processing approach well suited for FPGA implementation. HashCache is a hash-based state-tracking approach that combines high lookup, update, and insertion rates on arbitrary packet streams. It can be readily implemented on FPGA platforms equipped with off-the-shelf DDR4-SDRAM to hold billions of state entries but still operate at more than 100 million connections per second and memory channel. Moreover, HashCache is highly configurable and can be adjusted for specific needs on throughput, latency, or FIB resource utilization. We demonstrate HashCache with a physical setup that showcases 400G statefull firewalling under adverse conditions.

Title: Enclustra product roadmap
Presenter: Samir Jokar, Product Manager, Business Unit Standard Platforms, Enclustra GmbH, Switzerland
Abstract:
Coming

Title: Demo: Making a simple but structured VHDL testbench – for beginners
Presenter: Espen Tallakesen, TechSeed EmLogic, Norway
Time: 1 hour
Abstract:
This step-by-step demo is intended for designers and verification engineers who want to learn how to make better and more structured VHDL testbenches.
This session will show you what is needed for *any* good testbench, independent of complexity.
We will make a testbench from scratch for a simple VHDL module and do the following – using well documented VHDL procedures and functions from UVVM, an open source VHDL verification methodology, growing faster than any other FPGA verification methodology.

- Add a balanced and controllable clock generator
- Add logging of progress in a simple way
- Check default values and reset
- Access module via an interface – using BFMs (Bus Functional models)
- Check output signals with and without a positive acknowledge
- Wait for flag or interrupt or a given value – with a timeout
- Check that signals have been stable – without pulses or spikes for a given time
- Change verbosity to show different groups of messages in the transcript
- Report an alert summary
- … and more

The presented solution is using UVVM Utility Library and BFMs (also Open source), but the principles and mechanisms are 100% state of the art general verification methodology – independent of library.

Although this testbench is applied on a very simple DUT (Device Under Test), the same principles apply also to advanced testbenches for complex DUTs. (But the advanced testbenches need more on top.)

Title: VUnit integration into existing code base and leveraging verification components for better testbenches
Presenter: Sebastian Hellgren, CodeCache Linköping AB, Sweden
Abstract:
Enabling and standardizing automated tests for the large critical HVDC systems at Hitachi Energy is essential to catch errors early and avoiding large costs and delays during system level testing.
See how we integrated VUnit and TSFPGA in an existing codebase to enable build and test automation for a large number of projects.
In many projects, the FPGAs make heavy use of external components and interfaces. I will also describe how we used VUnit's verification component library to make testing of external interfaces better and easier.

Title: Functional Safety in FPGA Designs
Presenter: Martin Kellermann, Microchip Technology GmbH, Munich
Abstract:
Functional safety is a topic of rising importance, as its significance continues to grow with the increasing use of Field Programmable Gate Arrays (FPGAs) in these applications. In this session from Microchip will delve into the following topics:

- Defining safety and where it is applicable in the overall system.
- A systematic approach to designing a safe system.
- Key considerations in system design and FPGA selection

We will also be sharing insights on how clients are supported with information, including safety packages for various FPGAs and SoCs families. Supporting devices from the mid-range class of PolarFire® FPGA and SoC and also devices from our previous generations, which are still actively used in new projects. You will also learn about the safety considerations that must be taken into account to maintain safety in your designs. Don't miss this opportunity to deepen your understanding of functional safety and gain valuable insights from experts in the field.

Title: Introduction to Vector Processing and Neural Network Acceleration on Microchip FPGAs
Presenter: Brian Colgan, Microchip Technology GmbH, Dublin
Abstract:
Artificial Intelligence (AI) and Machine Learning (ML) are revolutionizing various industries, and the technology enabling them is becoming increasingly critical. These technologies are particularly useful for image, video, audio and signal processing. Microchip's VectorBlox™ Accelerator Software Development Kit (SDK) is a game changer in this area, as it offers the most power-efficient Convolutional Neural Network (CNN)-based AI/ML inference with PolarFire® FPGAs. Microchip's CoreVectorBlox IP is composed of a Matrix processor (MXP) and a CNN accelerator. The VectorBlox accelerator can support up to 279 GOP/s while being two to three times more power efficient than comparable solutions at the same performance. In this session, we will delve into the VectorBlox SDK and demonstrate how easy it is to get started using PolarFire FPGAs. Join us to explore the power and efficiency of VectorBlox accelerator for your AI/ML applications.

Title: Cross-vendor model-based RTL design with the OSS Whiznium developer tools
Presenter: Alexander Wirthmüller, MPSI Technologies GmbH, Germany
Abstract:
RTL design is time-consuming, making it important for developers to focus on the core functionality of their projects. The OSS Whiznium developer tools offer a user-extensible design approach covering auxiliary features such as host-FPGA communication with model-based source code generation. The concept extends to vendor-agnostic signal-level debugging in auto-generated web UI's and more. It is presented by example of a tabletop 3D laser scanner, implemented on all major FPGA(-SoC) platforms.

Title: IP replication and partial reconfiguration using an FPGA with 2D NoC
Presenter: Simon Longcroft, Achronix, USA
Abstract:
This session will discuss leveraging a 2-Dimensional Network-on-Chip (2D NoC), a repetitive logic cluster-based FPGA core-fabric hardware architecture, and a comprehensive software tools stack to:

- Create a soft IP core where all data and control inputs/outputs of the core can be connected to the 2D NoC via NoC Access Points (NAPs) inside each FPGA logic cluster, enabling the core to communicate with all IO and memory interfaces (such as PCIe, DDR4, GDDR6, Ethernet, etc.) and all other IP cores in the FPGA fabric that are also connected to the 2D NoC
- Compile, place-and-route, and close timing on the IP core once, in 1 location (placement) in the FPGA core fabric.
- Copy that IP core 1 to N times and move it to any location in the core fabric (up to 80 locations in AC7t1500). Copying and moving the IP core retains the complete place-and-route solution and timing closure regardless of location within the FPGA fabric.
- Generate a partial reconfiguration bitstream for the timing-closed IP core once in a single location (placement) in the FPGA core fabric.
- Use software bitstream remapping tools (TCL commands or PCIe API calls for on-the-fly remapping) to move the bitstream image from its original placement location to any relative location in the FPGA core fabric.
- Dynamically pipe dataflow between IP cores using the 2D NoC. The host/control system can send commands to re-direct data to different IP cores as part of the partial reconfiguration process by simply changing the target 2D NoC address.
- Create an IP marketplace that enables multi-tenancy solutions by instantiating and moving multiple IP cores from a mix of vendors to fill up the FPGA.
- Enable IP integration from a mix of 3rd party vendors and internal projects at various levels, including bitstreams. Customers can directly use the bitstream and the software bitstream remapping functions to drop IP directly into the core fabric in any location they choose.
- Enable data center dynamic load balancing of accelerator functions within a single FPGA. Examples will be presented.
- This presentation will walk through the solution's key concepts and technical details, referencing Achronix products as an example.

Title: Why are RISC-V® and TinyML a good path to scalable low power AI deployment at the Edge?
Presenter: Joachim Mueller, FAE Manager Europe, Efinix, USA
Abstract: RISC-V®, a well-known Instruction Set Architecture, generates more and more attention. For AI deployment at the edge the open-source community developed a TensorFlow Lite for Microcontrollers C++ Library running on RISC-V® as well. With Efinix TinyML Platform the FPGA vendor opens a path from TensorFlow Lite models developed for RISC-V® to scalable low power, small footprint FPGA implementations with custom acceleration options. TensorFlow, the TensorFlow logo and any related marks are trademarks of Google Inc.

Title: Abusing the VUnit test runner for FPGA build automation
Presenter: Ludvig Vidlid, Truestream AB, Sweden
Abstract: Unit tests are at the heart of VUnit, but the test runner is the brain. The ability to robustly run multiple jobs in parallel and get a nice report is handy in many situations outside of unit testing. See how we transplanted the VUnit test runner into tsfpga to control synthesis and run build size checkers, with an interface familiar to VUnit users.

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