08:30	**FPGAworld 2023** **Registration Sep 14th, DTU (SCION), Building 372, Diplomvej 2800 Lyngby**

Sponsors 2023

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09:00	**Conference opening** Professor Lars Dittmann, Technical University of Denmark, and Lennart Lindh, FPGAworld
09:15-10:00	**Keynote** **Title: RISC-V: Paving the Path Together to a Safe, Secure and Reliable Future** **Keynote speaker:** Martin Kellermann, Microchip Technology GmbH, Munich **Abstract:** RISC-V is an open-source instruction set that has created opportunities for companies of all sizes to innovate and make decisions independently. It is predicted to shape the future of computing for the next 50 years by providing a processor architecture that allows for more processing with a smaller carbon footprint, more features with less development resources, and new ways to combat threats with existing technologies. Companies are already utilizing RISC-V to develop applications such as High-Performance Spaceflight Computing (HPSC) processors. This keynote will explore how companies can benefit from this independence and how the ecosystems can enable easy adoption and scalability. It will also highlight companies that are already a part of this revolution and discuss how they can help create a safe and secure future. Through RISC-V, companies can reach their goals and protect their future. Together, we can move mountains. **CV:** Martin Kellermann is an experienced FPGA and SoC engineer with a diploma in Electrical Engineering from the Landshut University of Applied Sciences. He has expertise in high-speed serial data transmission, signal integrity, and hardware debugging, successfully delivering projects in the industrial, automotive, and data-center domains. As Marketing Manager at Microchip Technology GmbH, Munich, he works with the European Sales and Field Application team to showcase the strengths of their FPGAs and SoCs. **Session Chair:** Professor Lars Dittmann, Technical University of Denmark
10:00-10:30	**Coffee Break & Exhibition SPONSOR** XJTAG PCBA Testing & Programming
10:30-12:00 3*30 min	**Presentations** **Session Chair:** Lennart FPGAworld **Title:** New Intel FPGAs for mid-range applications **Presenter:** Mark Frost, Arrow/Intel, USA **Title:** Why are RISC-V® and TinyML a good path to scalable low power AI deployment at the Edge? **Presenter:** Joachim Mueller, FAE Manager Europe, Efinix Inc **Title:** Lattice Avant, a new level of low power FPGA innovation for mid-range applications. **Presenter:** Paul Hardy, Senior Applications Engineering Lattice, Europe.

12:00-13:00	**Lunch Break & Exhibition**
13:00-14:30 3*30 min	**Presentations** **Session Chair:** Lennart FPGAworld **Title**: Introduction to Vector Processing and Neural Network Acceleration on Microchip FPGAs **Presenter**: Brian Colgan, Microchip Technology GmbH, Dublin **Title:** FPGA and board design patterns to aid (MTBF and) SEU-aware loss-of-function quantitative estimates. **Presenter:** Cristian Ciressan, Enclustra GmbH, Switzerland More_information **Title:** IP replication and partial reconfiguration using an FPGA with 2D NoC **Presenter:** Simon Longcroft, Achronix, USA More information
14:30-15:00	**Coffee Break & Exhibition**
15:00-16:30 3*30 min	**Presentations** **Session Chair:** Lennart FPGAworld **Title**: Functional Safety in FPGA Designs **Presenter**: Martin Kellerman, Microchip Technology GmbH, Munich **Title:** Hanling asynchronous reset in multiple-clock synchronous FPGA systems **Presenter:** Dr. Reuven Dobkin, CTO of vSync Circuits **Title:** 10 years of FPGA SoM's **Presenter:** Antti Lukats, Trenz Electronic GmbH, Germany More_information
16:30 -	**Go Home Drink in Exhibition Hal**

Sponsors, exhibitors and/or presenters Copenhagen and Stockholm	DTU, Technical University of Denmark AFRY, Sweden Aktuel Elektronik, Denmark AGSTU FPGA Education, Sweden XJTAG, UK Microchip, UK Intel PSG, USA Efinix, USA Truestream AB, Sweden MathWorks, USA	Achronix, USA Lattice Semiconductor, USA Synective Labs, Sweden SynoGate, Germany Emlogic, Norway Enclustra GmbH, Switzerland Avnet Silica, Denmark BitSim NOW, Sweden Trenz Electronic GmbH, Germany MathWorks, USA	CodeCache Linköping AB, Sweden MPSI Technologies GmbH, Germany Arrow, Europe Avnet Silica, Sweden XPERI, USA VSYNC, Israel Motion Control, Sweden FPGAworld, Sweden

More information

Keynote Speakers Copenhagen

Title: RISC-V: Paving the Path Together to a Safe, Secure and Reliable Future

Keynote speaker: Martin Kellermann, Microchip Technology GmbH, Munich

Abstract: RISC-V is an open-source instruction set that has created opportunities for companies of all sizes to innovate and make decisions independently. It is predicted to shape the future of computing for the next 50 years by providing a processor architecture that allows for more processing with a smaller carbon footprint, more features with less development resources, and new ways to combat threats with existing technologies. Companies are already utilizing RISC-V to develop applications such as High-Performance Spaceflight Computing (HPSC) processors. This keynote will explore how companies can benefit from this independence and how the ecosystems can enable easy adoption and scalability. It will also highlight companies that are already a part of this revolution and discuss how they can help create a safe and secure future. Through RISC-V, companies can reach their goals and protect their future. Together, we can move mountains.

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Presentations with abstracts

Title: Hanling asynchronous reset in multiple-clock synchronous FPGA systems
Presenter: Dr. Reuven Dobkin, CTO of vSync Circuits

Abstract:
Asynchronous resets are traditionally employed in VLSI designs for bringing synchronous circuitry to a known state after power up. Asynchronous reset release operation must be coordinated with the synchronous logic clock signal to eliminate synchronization failures due to possible contention between the reset and the clock (a.k.a. recovery/removal timing violations). A lack of such coordination leads to intermittent failures on power up. During the lecture we will review FPGA implementation approaches for asynchronous reset hanling and synchronization.

Title: Lattice Avant, a new level of low power FPGA innovation for mid-range applications.
Presenter: Paul Hardy, Senior Applications Engineering Lattice, Europe.
Abstract:
Lattice Avant is a new FPGA platform purpose-built to bring the Lattice's power efficient architecture, small size, and performance leadership to mid-range FPGAs. Explore Avant's features, that offer best-in-class power efficiency, advanced connectivity, and optimized compute, all in a small footprint. Find out how the design choices for Avant architecture resulted in power and performance optimizations. Learn about the Avant-E family and portfolio of development tools to get you started on developing with Avant.

Title: New Intel FPGAs for mid-range applications
Presenter: Mark Frost, Arrow/Intel, USA
Abstract:

The wait is finally over! Intel PSG has a new roadmap for mid-range FPGAs, ideally suited to video, vision and broadcast applications. Attend this short session to gain an overview of this brand new mid-range FPGA product, an addition to the cutting-edge Agilex family.

Title: FPGA and board design patterns to aid (MTBF and) SEU-aware loss-of-function quantitative estimates.
Presenter: Cristian Ciressan, Enclustra GmbH, Switzerland
Abstract:
For Safety-Critical applications, trying to estimate the loss-of-function (LoF) probability during mission time, when using COTS boards, is a creative process to say the least.
Certain assumptions are made, followed by an often ad-hoc analysis to eventually get the desired quantitative figure(s). Whether the process followed, and the results generated are accepted or not, ultimately depends on a certification authority.
We will talk about (1) a proposed formalism to address the task of (MTBF and) SEU-aware LoF estimation, (2) how this formalism is translated to certain FPGA and board design patterns and (3) provide examples of how this is applied in a few practical situations.

Title: 10 years of FPGA SoM's
Presenter: Antti Lukats, Trenz Electronic GmbH, Germany
Abstract:
Brief history of 10+ years of FPGA SoM development; challenges and design choices. Technology showcase SoM's, customer driven SoM's. Legacy/standard issues. Break-out style SoM's. Successes and failures.

Title: Functional Safety in FPGA Designs
Presenter: Martin Kellermann, **Microchip Technology GmbH, Munich**
Abstract:
Functional safety is a topic of rising importance, as its significance continues to grow with the increasing use of Field Programmable Gate Arrays (FPGAs) in these applications. In this session from Microchip will delve into the following topics:

- Defining safety and where it is applicable in the overall system.
- A systematic approach to designing a safe system.
- Key considerations in system design and FPGA selection

We will also be sharing insights on how clients are supported with information, including safety packages for various FPGAs and SoCs families. Supporting devices from the mid-range class of PolarFire® FPGA and SoC and also devices from our previous generations, which are still actively used in new projects. You will also learn about the safety considerations that must be taken into account to maintain safety in your designs. Don't miss this opportunity to deepen your understanding of functional safety and gain valuable insights from experts in the field.

Title: Introduction to Vector Processing and Neural Network Acceleration on Microchip FPGAs
Presenter: Brian Colgan, **Microchip Technology GmbH,** Dublin
Abstract:
Artificial Intelligence (AI) and Machine Learning (ML) are revolutionizing various industries, and the technology enabling them is becoming increasingly critical. These technologies are particularly useful for image, video, audio and signal processing. Microchip's VectorBlox™ Accelerator Software Development Kit (SDK) is a game changer in this area, as it offers the most power-efficient Convolutional Neural Network (CNN)-based AI/ML inference with PolarFire® FPGAs. Microchip's CoreVectorBlox IP is composed of a Matrix processor (MXP) and a CNN accelerator. The VectorBlox accelerator can support up to 279 GOP/s while being two to three times more power efficient than comparable solutions at the same performance. In this

session, we will delve into the VectorBlox SDK and demonstrate how easy it is to get started using PolarFire FPGAs. Join us to explore the power and efficiency of VectorBlox accelerator for your AI/ML applications.

Title: Why are RISC-V® and TinyML a good path to scalable low power AI deployment at the Edge?
Presenter: Joachim Mueller, FAE Manager Europe, Efinix, USA
Abstract: RISC-V®, a well-known Instruction Set Architecture, generates more and more attention. For AI deployment at the edge the open source community developed a TensorFlow Lite for Microcontrollers C++ Library running on RISC-V® as well. With Efinix TinyML Platform the FPGA vendor opens a path from TensorFlow Lite models developed for RISC-V® to scalable low power, small footprint FPGA implementations with custom acceleration options. TensorFlow, the TensorFlow logo and any related marks are trademarks of Google Inc.

Title: IP replication and partial reconfiguration using an FPGA with 2D NoC
Presenters Name: Simon Longcroft, Achronix, USA
Abstract:
This session will discuss leveraging a 2-Dimensional Network-on-Chip (2D NoC), a repetitive logic cluster-based FPGA core-fabric hardware architecture, and a comprehensive software tools stack to:

- Create a soft IP core where all data and control inputs/outputs of the core can be connected to the 2D NoC via NoC Access Points (NAPs) inside each FPGA logic cluster, enabling the core to communicate with all IO and memory interfaces (such as PCIe, DDR4, GDDR6, Ethernet, etc.) and all other IP cores in the FPGA fabric that are also connected to the 2D NoC
- Compile, place-and-route, and close timing on the IP core once, in 1 location (placement) in the FPGA core fabric.
- Copy that IP core 1 to N times and move it to any location in the core fabric (up to 80 locations in AC7t1500). Copying and moving the IP core retains the complete place-and-route solution and timing closure regardless of location within the FPGA fabric.
- Generate a partial reconfiguration bitstream for the timing-closed IP core once in a single location (placement) in the FPGA core fabric.
- Use software bitstream remapping tools (TCL commands or PCIe API calls for on-the-fly remapping) to move the bitstream image from its original placement location to any relative location in the FPGA core fabric.
- Dynamically pipe dataflow between IP cores using the 2D NoC. The host/control system can send commands to re-direct data to different IP cores as part of the partial reconfiguration process by simply changing the target 2D NoC address.
- Create an IP marketplace that enables multi-tenancy solutions by instantiating and moving multiple IP cores from a mix of vendors to fill up the FPGA.
- Enable IP integration from a mix of 3rd party vendors and internal projects at various levels, including bitstreams. Customers can directly use the bitstream and the software bitstream remapping functions to drop IP directly into the core fabric in any location they choose.
- Enable data center dynamic load balancing of accelerator functions within a single FPGA. Examples will be presented.

This presentation will walk through the solution's key concepts and technical details, referencing Achronix products as an example.

Thank you Sponsors!

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