08:30	**FPGAworld, 13 September 2022** **Registration**: Stockholm, AFRY, Frösundaleden 2A, 169 70 Solna, SWEDEN		
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09:00	**Conference Opening** Jihad Daoud, AFRY and Lennart Lindh, FPGAworld **Room:** Devoted 09		
09:15-10:00	**Keynote** **Title: FPGAs for Deep Learning applications – Trends, solutions, and tools** **Keynote speaker:** Magnus Peterson, Synective labs, Sweden **Room:** Devoted 09 **Abstract:** This talk will look at the current trends and present different ways of implementing Deep Learning inference on FPGAs. It will also walk you through the different approaches taken by the different FPGA vendors and their different deep learning toolsets. **Session Chair:** Jihad Daoud, AFRY		
10:00-10:30	**Coffee Break & Exhibition**		
10:30-12:00 3*30 min	**Track** **Session Chair:** Tommy Klevin, AFRY **Room:** Devoted 09	**Track** **Session Chair:** Tobias Karlsson, AFRY **Room:** Devoted 04	**Track** **Session Chair:** Kim Petersén, HDC **Room:** Brave 05
	Title: Deep Learning Network Quantization for FPGA Deployment **Presenter:** Daniel Aronsson, MathWorks, USA **Title: DeepHLS v.2: Automating high-performance Deep Neural Network implementation on FPGA using High-Level Synthesis** **Presenter:** Mohammad Riazati, Mälardalen University, Sweden ~~**Title: Video Connectivity with Interface Bridge FPGAs in EVs and Automotive**~~ ~~**Presenter:** Grant Jennings, Gowin Semiconductor, China/US~~	**Title: Maximize External Memory Bandwidth Efficiency with Any Access Pattern** **Presenter:** Raymond Nijssen, VP and Chief Technologist, Achronix, USA **Title: Efficient and flexible path to implement hardware/software interfaces** **Presenter:** Bernd Röckert, Eccelerators GmbH, Austria **Title: PolarFire® SoC, differentiated application-class embedded processing** **Presenter:** Martin Kellermann, Microchip Ltd, UK	**Title: Zero-effort RTL bugs handling** **Presenter:** Dr. Reuven Dobkin, CTO of vSync Circuits, Israel **Title: Python and the art of building a high-quality reusable verification environment.** **Presenter:** Faïçal Chtourou, Field Application Engineer, Digital Verification Technologies, Siemens EDA (for InnoFour BV) **Title: Constrained Random & Functional Coverage for VHDL verification - understandable for anyone.** **Presenter:** Espen Tallaksen, TechSeed EmLogic, Norway
12:00-13:00	**Lunch Break & Exhibition**		
13:00-14:30 3*30 min	**VUnit Track** **Session Chair:** Lars Asplund, Synective labs Room: Devoted 09	**Track** **Session Chair:** Hasse Starck, AGSTU Room: Devoted 04	**Track** **Session Chair:** Kim Petersén, HDC Room: Brave 05
	Title: Automated HDL Verification with VUnit **Presenters:** Mikael Wetterholm, AGSTU/ Higher Vocational Education, Sweden **More information** **Titel: VUnit + Bazel**	~~**Title: Programming and Configuration Challenges in Volume Production Products**~~ ~~**Presenter:** Grant Jennings, Gowin Semiconductor, China~~	**Title: Demystifying security with Intel FPGAs: device & platform level** **Presenter:** Nikolay Rognlien, Arrow Electronics, Norge

	Presenters: Oskar Solsjö, Sylog, Sweden **Titel: Bridging HW and SW verification with VUnit co-simulation** **Presenters:** Unai Martinez-Corral, Antmicro and University of the Basque Country	**Title: How to cut development time through automation with CI/CD** **Presenter:** Andrew Swirski, Beetlebox, UK **Title: Efficient FPGA-based DSP – from KS/s up to GS/s** **Presenter:** Oliver Bründler, Enclustra GmbH, Switzerland	**Title: RISC-V® on Intel® FPGA** **Presenter:** Nikolay Rognlien, Arrow Electronics, Norge **Title: Low power, small footprint embedded vision solutions** **Presenter:** Brian Colgan, Microchip Ltd, UK
14:30-15:00	**Coffee Break & Exhibition**		
15:00-15:29	**Track** **Session Chair:** Hasse Starck, AGSTU **Room:** Devoted 09	**Track** **Session Chair:** Kim Petersén, HDC **Room:** Devoted 04	**Track** **Session Chair:** Tobias Karlsson, AFRY **Room:** Brave 05
	Title: Post-Quantum Cryptography and the Added Vallue of FPGAs **Presenter**: Tommi Lampila, Xiphera Oy, Finland	**Title: Turning IP cores into systems with FuseSoC** **Presenter:** Olof Kindgren, Qamcom Research & Technology, Sweden	**Title: Efficient multiple-clock design methodology** **Presenter:** Dr. Reuven Dobkin, CTO of vSync Circuits, Israel
	1 min walk to the room Devoted 09		
15:30-16:15	**Keynote** **Title: Challenges we face in achieving FPGA safety and security** **Keynote speaker:** Adam Taylor, Adiuvo, England **Room:** Devoted 09 **Abstract:** The keynote will discuss the challenges we face in achieving safety and security on budget and schedule, and what are the key challenges which face us technical, personal, and community. How can we work together as a community to develop education, frameworks, and approaches which enable safety and security to be addressed in our developments? **Session Chair:** Lennart Lindh, FPGAworld/AGSTU		
16:15 -	**Go Home Drink in the Exhibition Hall**		
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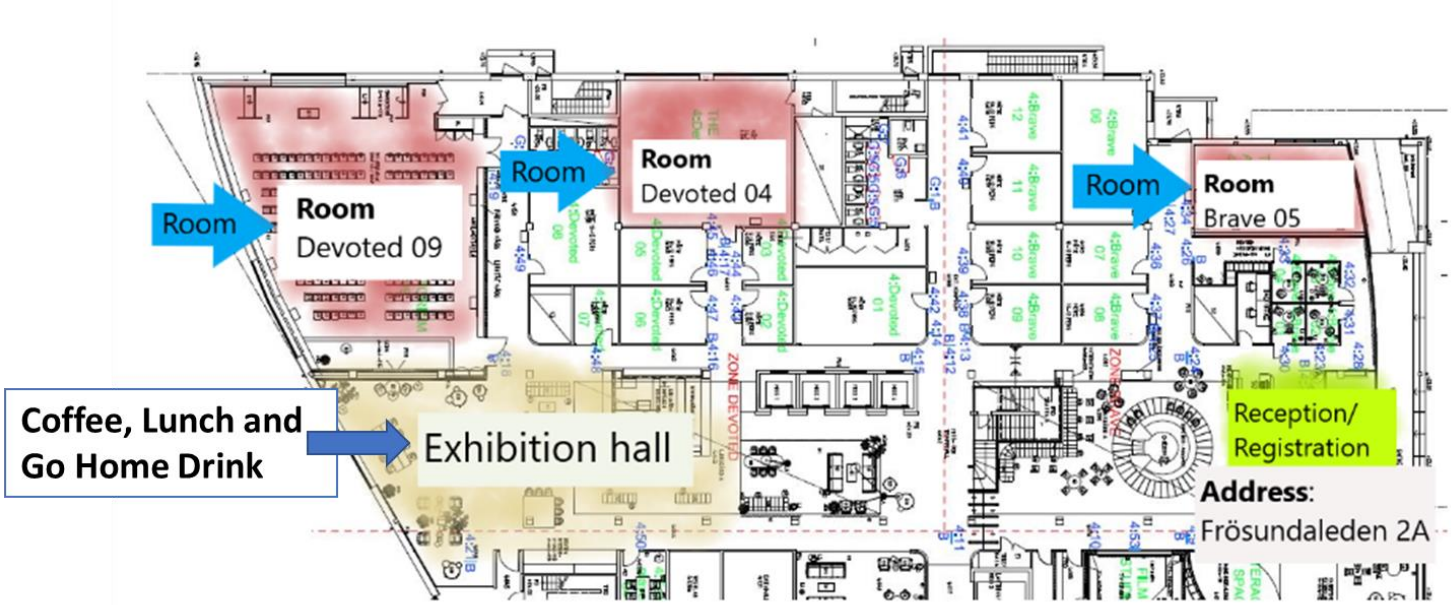

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Keynote Speaker Stockholm
Keynote Title: FPGAs for Deep Learning applications – Trends, solutions, and tools
Keynote speaker: Magnus Peterson, Synective Labs AB, Sweden
Abstract: Deep Learning has over the last years become a game-changer in many fields, adding extraordinary capabilities to systems and products. With strong competition from other technologies, FPGAs are in many cases a leading candidate platform for deep learning implementation, combining high-performance, low power, and high flexibility. Seeing new high-volume opportunities, like automotive vision applications, the FPGA vendors have put large efforts into developing streamlined design flows for easy integration of deep learning inference engines into an FPGA design. This talk will look at the current trends and present different ways of implementing Deep Learning inference on FPGAs. It will also walk you through the different approaches taken by the different FPGA vendors and their different deep learning toolsets.
About the presenter: Magnus has more than 35 years of experience in developing high-performance embedded solutions, mainly within vision and image processing, where FPGAs play a key role. He has been with Synective Labs since 2003 and worked previously with vision-based industrial inspection systems at Innovativ Vision AB.

Keynote Title: Challenges we face in achieving FPGA safety and security
Keynote speaker: Adam Taylor, Adiuvo Engineering, England
Abstract: According to the Wilson Group survey 84% of FPGA designs are released into the field with a non-trivial bug, in safety or security applications it can lead to injury, death, environmental impact, or a significant security breach. FPGAs are increasingly used for “commercial” applications such as IoT, autonomous driving, medical, and fintech. Worryingly only 52% of designs consider implementing security features and worse only

47% implement a safety-critical design.
The keynote will discuss the challenges we face in achieving safety and security on budget and schedule, and what are the key challenges which face us technical, personal, and community. How can we work together as a community to develop education, frameworks, and approaches which enable safety and security to be addressed in our developments?
About the presenter: Adam is a Chartered Engineer, Senior Member of the IEEE, Fellow of the Institute of Engineering and Technology, Visiting Professor of Embedded Systems at the University of Lincoln and Arm Innovator, Edge Impulse Ambassador, he is also the owner of the engineering and consultancy company Adiuvo Engineering and Training which develops embedded solutions for high reliability, mission-critical and space applications. Current projects include ESA Plato, Lunar Gateway, Generic Space Imager, UKSA TreeView, and several other clients across the world.
FPGAs are Adam‘s first love, he is the author of numerous articles and papers on electronic design and FPGA design including over 440 blogs and 30 million-plus views on how to use the Zynq and Zynq MPSoC for Xilinx.

Presentations

Title: Deep Learning Network Quantization for FPGA Deployment
Presenter: Daniel Aronsson, FPGA/ASIC Technical Expert, MathWorks
Abstract:
You have your trained deep neural net. Now what do you do to get it onto your FPGA board? In this presentation, we start with a trained net and show how to quantize it to fixed-point by using Fixed-Point Designer. Once we have verified that the quantized net performs as well as the original, we will then use Deep Learning HDL Toolbox to automatically deploy and test the net on a ZCU102 UltraScale+ board, directly from the MATLAB prompt.

Title: Efficient and flexible path to implement hardware/software interfaces
Presenter: Bernd Röckert, Eccelerators GmbH, Austria
Abstract:
All designs require communication between HW and SW.
This interface is often already planned in the concept phase and accompanies the project until the final product. Therefore, this point is a very important part of the development. Unfortunately, it often happens that because of project pressure the quality of it suffers. Because what was defined in a concept phase may later turn out to be not ideal or practical. But a change during the project development is often rejected with "too much effort", "what if when something goes wrong" or "then I have to change all other files like documentation or test, too". And exactly here the interface description language HxS helps you. It offers you the possibility to change the registers at any time with maximum flexibility without sacrificing quality.
HxS includes a generator for several output formats such as HDL, SW, test and documentation files. Thus, for each member of the project, the corresponding files are automatically recreated. This also allows everyone work on the same version. Copy and paste errors are also eliminated.
The unique interface description (HxS) also offers the possibility to use different domain structures. With this domain structure you can easily create your own library. Which allows the reuse of existing interfaces and improves the collaboration in the team.
In this presentation I would like to give you an insight into our HxS interface description.
Presenters Bio:
Bernd is one of the four founding members of Eccelerators GmbH. He started his engineering career in the field of FPGA development in 2015 after his successful master's degree at the University of Applied Sciences in Augsburg as an electrical engineer. Since then, he also expanded his FPGA area of expertise there to include the topic of regression testing on real HW, as well as everything related to DevOps itself. During this time, he also continued his education in the area of SW development. In the company Eccelerators he is active in the area of SW development and testing.

Title: Maximize External Memory Bandwidth Efficiency with Any Access Pattern
Presenter: Raymond Nijssen, VP and Chief Technologist, Achronix, USA
Abstract:
Increasingly, high performance compute engines with extreme demands on external DRAM bandwidth efficiency are implemented using FPGAs. Many applications require high sustained memory bandwidths and deterministic, low transaction latencies. While this can be achieved relatively easily where memory access patterns are long bursts with predictable addresses, it is very challenging with applications that have random inherent address access patterns. This includes applications like GNNs in AI/ML, large key-value-store in SmartNICs, and DAG traversal in cryptocurrency mining. If this problem is not addressed, the effective memory bandwidth efficiency can drop below 25% of the memory subsystem's capabilities. For example, in case of an aggregate 4Tbps peak bandwidth GDDR6 system, that means only 1Tbps. Since memory access efficiency is the bottleneck of these applications, the entire system's performance can end up being a fraction of its product requirement. This is largely due to the internal architecture consisting of ranks, banks, groups, rows, and columns in all DRAM technologies like HBM2/3, GDDR6 and (LP)DDR4/5. Its many complex timing constraints make it difficult for designers to accurately assess overall performance of their system. Memory controllers in modern FPGAs have advanced features to minimize these impacts like reorder queues and programmable dynamic scheduling strategies. Advanced FPGA macro-architectures provide hardened high bandwidth data transport features to remove the burden of having to weave super-wide high frequency data busses throughout their design. This presentation details how to manage these limitations and leverage these features so that the effective DRAM bandwidth efficiency can be close to the theoretical upper limit, even with worst-case access patterns. It showcases how this can be easily achieved with practical FPGA designs using the GDDR6 memory subsystem and the high bandwidth 2D NOC architecture in Achronix Speedster7t FPGAs.

Presenters Bio:
Mr. Nijssen has over 20 years of experience in the FPGA and EDA industries in various technical and management positions. Mr. Nijssen joined Achronix as Chief Software Architect to manage the software development group, define the foundations and algorithms of the software system, and architect key aspects of the company's FPGA architectures. In his current role, he is responsible for the productization of the company's current products and R&D for new technologies for future products. Prior to Achronix, Mr. Nijssen was at Tabula where he was responsible for placement and timing analysis of a time-multiplexed FPGA technology. Prior to Tabula, he was one of the first engineers at Magma Design Automation, and held multiple leadership positions in charge of routing and placement, data models and customer deployment of Magma's Blast Plan Pro hierarchy hierarchical virtual prototyping and floorplanning products for very large ASIC designs. Mr. Nijssen received his MSEE degree from Eindhoven University of Technology in The Netherlands, and after that followed its postgraduate program studying EDA for VLSI. He holds several patents related to P&R and asynchronous circuit technologies.

Title: Efficient FPGA-based DSP – from kS/s up to GS/s
Presenter: Oliver Bründler, FPGA/SoC System Design Expert, Enclustra GmbH, Switzerland
Abstract:
With increasing bandwidth requirements in wireless systems and RFSoCs, including multi-GS/s converters, Digital Signal Processing (DSP) techniques must evolve to support sample rates beyond the clock frequency that the FPGA fabric can achieve. At the same time, there are also applications where much lower sample rates are sufficient, and the focus is on resource- and effort-efficient implementation. In this talk, we will discuss how to meet these challenges. We will present our Universal DSP Library, which minimizes development time for lower sample rates (up to the clock frequency). Then we will focus on the design, implementation and analysis of parallel DSP blocks capable of processing several gigasamples per second. A short presentation of the Enclustra plug-and-play SoC modules and our profound FPGA expertise and services rounds off the talk.

Title: Python and the art of building a high-quality reusable verification environment.
Presenter: Faïçal Chtourou
Field Application Engineer, Digital Verifcation Technologies, Siemens EDA (for InnoFour BV)

Abstract:
Constrained randomization and functional coverage have recently become crucial elements to a successful tape out. SystemVerilog and UVM framework is the de-facto standard for verification. Still, due to a high learning time/benefit ratio, many users preferred to look into other alternatives such as UVVM/OSVM.
Lately, Python has emerged as a third option, and it is gaining interest for its obvious advantages (easy language, big community, extensive library …). The purpose of this presentation is to show you how we can build a high-quality reusable verification environment using Python Libraries/Framework.

Title: PolarFire® SoC, differentiated application-class embedded processing
Presenter: Martin Kellermann, Microchip Ltd, UK
Abstract:
Many applications today suffer from constraints on size, power and thermal capabilities. Microchip PolarFire® SoC devices, based on 64-bit quad-core RISC-V application processors, tackle these constraints and allow users to approach and build applications often deemed impossible. The presentation will explain the background on why PolarFire devices solve many of the challenges in such applications as vision or communication-based designs and will show use-cases of designs only made possible by small form factor, low-power FPGAs.

Title: Low power, small footprint embedded vision solutions
Presenter: Brian Colgan, Microchip Ltd, UK
Abstract:
Miniaturization is a key feature in most embedded systems today. Consumers want more computing power in their pockets. Most FPGA-based vision systems are also following the same trend. Consumers want smaller industrial and professional cameras, medical handhelds, or thermal imaging systems, to name a few applications.
Miniaturization also poses additional challenges—the biggest one can be condensed into a single term "power-efficient performance". Typically, if a system's performance goes up, its power consumption does too, which in-turn increases heat dissipation. And in smaller modules, heat dissipation is a system headache designers cope with every day. Cooling a module so that it can operate under a thermally-constrained environment often becomes the bottleneck to performance.
Microchip will show solutions to address this headache by through highly=power-efficient FPGAs and SoCs in smart embedded vision applications. This session will give an overview of how to utilize the architecture of Microchip's PolarFire® FPGAs and SoCs to build high resolution cameras in severely space- and temperature-constrained housings. The session will also address how machine learning can be added using both FPGAs and SoCs and what design- and development vehicles are available.
Additionally, a small example will show how to add security to these applications using the built-in architecture features of the PolarFire FPGA-based SoC.

Titel: Automated HDL Verification with VUnit
Presenters: Mikael Wetterholm, AGSTU/ Higher Vocational Education, Sweden
Abstract:
VUnit is a tool for automated verification tasks, easy to adopt, and open source. The presentation gives a brief introduction to VUnit and share the experience through two completed projects. One with a simple timer and one with a complex real-time kernel in hardware.

Titel: VUnit + Bazel
Presenters: Oskar Solsjö, Sylog, Sweden
Abstract:
HDL development can sometimes be seen as something of an odd bird in the SW CI pipeline. Its toolchains and artifacts often times being proprietary, not (incrementally) buildable and flaky (e.g., congestion in synthesis). Integration with the rest of the SW CI pipeline can also be easily hampered due to it requiring: - Domain knowledge - Resources in compute (builds take a lot of resources) - Resources in time (builds taking a lot of

time, long running tests) - Cost in setup / configuration of CI, toolchains. What does the HDL developer want? Quick feedback, testing early and as much as possible. How then can we make the HDL development odd bird fly in harmony with rest of bird flock. Meet the acylic dependency graph, meet build and test caches, meet VUnit + Bazel.

Titel: Bridging HW and SW verification with VUnit co-simulation
Presenters: Unai Martinez-Corral, Antmicro and University of the Basque Country
Abstract:
In SoCs comprising CPUs and custom accelerators, communication is typically handled through standardised interfaces. However, software and hardware are developed and tested by different people/teams. Verification Components (VCs) provide a bridge between both domains; on the one hand, they have a hardware interface with ports/signals; and, on the other hand, they provide a software API to interact with those. VUnit provides Verification Components written in plain VHDL 2008. These are friendly for hardware designers, but might feel awkward for software developers. Direct Co-Simulation allows to close the gap, by binding the software APIs in VHDL to functions written in C, Python, m, etc. In this presentation, we will go through various examples using VUnit, Verification Components and GHDL to co-simulate VHDL hardware and any other language satisfying C calling conventions. Since all the tools and the sources are FLOSS, we will use Continuous Integration (CI) services such as GitHub Actions or GitLab CI/CD to make the best of co-simulation and Test Driven Development (TDD).

Title: Demystifying security with Intel FPGAs: device & platform level
Presenter: Nikolay Rognlien, Arrow Electronics, Norge
Abstract:
FPGA device security can be a complex and overwhelming area for system architects and FPGA designers, with many opting to skip even basic security measures in their products. It doesn't have to be and shouldn't be this way; with many examples of vulnerabilities in products, security has never been more important. Intel FPGAs have some new security features which aim to make implementing security much easier.
The presentation will cover areas such as: Security attributes and attack vectors, Authentication, Encryption/Decryption, Vendor Authorised Boot, Attestation, Black Key Provisioning, and Crypto Services. The aim is to give a technical overview of each topic, why it is valuable to the audience and how to implement in Intel FPGAs

Title: How to cut development time through automation with CI/CD
Presenter: Andrew Swirski, Beetlebox, UK
Abstract:
FPGA development is in a crisis. 68% of FPGA projects were behind schedule in 2020 and only 17% of FPGA projects had no bugs escape into production, according to Wilson Research Group. How can we get projects completed on time and error free even as our chips become larger and more advanced? The answer is automation. In this presentation we will explore how teams can automate their processes through CI/CD (Continuous Integration/ Continuous Delivery) using Beetlebox's new tool BeetleboxCI.

Title: RISC-V® on Intel® FPGA
Presenter: Nikolay Rognlien, Arrow Electronics, Norge
Abstract:
The RISC processor architecture has a long history and since its very beginnings as the "Berkeley RISC" in 1981 it has gone through various architecture generations. In 2010 the first RISC-V® implementation came to live at UC Berkeley and meanwhile this has emerged quite significantly. Today, different variants of 32-/64-/128-bit architectures exist, and the specification continues to be developed. The list of members in the RISC-V® organization is quite long and there are a few silicon devices and development boards available from different sources now.

Intel® who is a Premium Member of the RISC-V® organization does have a RISC type soft processor called NIOS® II which is used in the Intel® FPGAs already for more than a decade. Although Nios® II is highly versatile and configurable, it uses its own proprietary instruction set and tools.
Now Intel® has emerged its soft processor portfolio and started to ship the new FPGA soft processors called Nios® V/m which has a RISC-V® RV32IA compatible architecture. This not only enables much higher performance compared to the Nios® II but also allows to utilize the huge RISC-V® infrastructure and eco-system.
During this session, we will look at the architecture and configuration options of the Nios® V/m core compared to the Nios® II processor version. We will investigate the hardware/software development and debugging flows as well as the usable eco-system.

Title: Turning IP cores into systems with FuseSoC
Presenter: Olof Kindgren, Qamcom Research & Technology
Abstract:
In many ways, HDL developers have been years behind their counterparts in the software world. One such area is core management. Where the software developers simply specify which libraries they depend on, HDL developers rely on copying around source code. Where software developers can select their build tool with a command-line switch, HDL developers use tool-specific project files powered by custom makefiles. FuseSoC rectifies this by bringing modern software practices in the shape of a package manager and a uniform build system to HDL developers, making it easy to reuse existing code, change tools and move projects between FPGAs from different vendors. Having been around for over ten years there are now hundreds of FuseSoC-compatible cores and more than 30 different simulation, synthesis and lint tools supported. This presentation will give an overview of where FuseSoC can help spending less time on the cores, and more time on the core business.

Title: Programming and Configuration Challenges in Volume Production Products
Presenter: Grant Jennings, Gowin Semiconductor, China/US
Abstract:
While programming a bitstream into an FPGA may seem trivial there has been over 30 years of programming utilities developed by FPGA manufacturers and their customers. These utilities often support non-standardized features and customers require a high resistance to production line changes. Legacy FPGA's have programming interfaces with severe limitations in terms of speed, configurability, and compliance. This presentation will walk through many observations and solutions found from customers attempting production after switching to new FPGA manufacturers.
Bio:
Grant Jennings is the Director of International Marketing for Gowin Semiconductor focused on strategic solutions for programmable technologies. He has over 15 years of FPGA systems architecture experience in areas including ASIC prototyping, interfacing, bridging and edge connectivity. Jennings received his electrical engineering degree from Iowa State University and his MBA from Texas A&M University.

Title: Video Connectivity with Interface Bridge FPGAs in EVs and Automotive
Presenter: Grant Jennings, Gowin Semiconductor, China/US
Abstract:
Video paths around a vehicle are exponentially increasing due to technology advancements in digital gauges, infotainment, car/driver recorders, ADAS and vehicle surveillance. Adapting video streams throughout the vehicle creates extreme electrical interface, power and processing challenges, which must be balanced with reliability, cost and power for the semiconductor components required. Automotive FPGAs have become a leading solution for interfacing, bridging and processing automotive systems supporting both legacy and upcoming video interfaces such as MIPI A-PHY, D-PHY, C-PHY, CSI-2 and DSI.
This presentation will discuss how FPGAs are being used to merge, mux, split convert and process multiple video streams in modern automotive applications.

Title: Zero-effort RTL bugs handling
Presenter: Dr. Reuven Dobkin, CTO of vSync Circuits, Israel
Abstract:
RTL bugs are traditionally discovered using dynamic simulation, consuming time, and requiring high effort to achieve a satisfying coverage. During this lecture we will review common bugs that may appear in a few popular RTL implementation approaches for FSMs, reset logic, bus logic, and more. We will show how these bugs can be automatically identified and reported, without running the simulation, thus significantly reducing the verification effort.

Title: Efficient multiple-clock design methodology
Presenter: Dr. Reuven Dobkin, CTO of vSync Circuits
Abstract:
Clock domain crossing (CDC) issues are a common reason for random failures of FPGA and ASIC designs. During this lecture we will review a few common CDC failure examples and will discuss how such bugs can be avoided or discovered using the proposed design and verification tool-based methodology. In addition, we will show how third-party vendor IPs can be effectively handled in the light of the same methodology.

Title: Constrained Random & Functional Coverage for VHDL verification - understandable for anyone.
Presenter: Espen Tallaksen, TechSeed EmLogic AS, Norway
Abstract:
UVVM - the VHDL Verification Methodology, has been extended with advanced constrained randomization and functional coverage - with syntax and naming that eases the understanding significantly. With this improved functionality, anyone can write complex constraints to improve the verification quality.
This presentation will show how this works and explain how you can get started in a very simple way.

Title: DeepHLS v.2: Automating high-performance Deep Neural Network implementation on FPGA using High-Level Synthesis
Presenter: Mohammad Riazati, Company/school/university: Mälardalen University, Sweden
Abstract:
FPGA implementation of Deep Neural Networks is challenging for neural network designers since they usually have limited knowledge of hardware. We propose an automatic toolchain to use High-Level Synthesis (HLS) for this purpose. Firstly, a fully automated tool for creating a synthesizable C implementation from Keras is created. Then, since HLS only transforms a C implementation, and the parallelism capability of a device is not utilized, HLS directives are found through a two-stage design space exploration to create a high-performance implementation with minimal latency.

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