08:30	**FPGAworld 15 September 2022** **Registration:** DTU (SCION), Building 372, Diplomvej 2800 Lyngby
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09:00	**Conference opening** Professor Lars Dittmann, Technical University of Denmark, and Lennart Lindh, FPGAworld
09:15-10:00	**Keynote** **Title:** Post-Quantum Cryptography and the Added Vallue of FPGAs **Keynote speaker:** Matti Tommiska, Xiphera Ltd, Finland **Abstract:** If large-scale quantum computers could be built, they would be able to solve the hard mathematical problems that are the basis of the current public-key cryptography. Consequently, quantum computing poses a serious threat to the security of the Internet. Post-Quantum Cryptography (PQC) refers to cryptographic algorithms that can be implemented on traditional computing platforms - such as FPGAs - but are based on mathematical problems that remain secure even against quantum attacks. This talk reviews the status of PQC and discusses how the reprogrammability of FPGAs adds value during the multi-year transition period from classical algorithms to PQC. **CV:** Matti has worked with FPGAs since 1995, when he started working as a researcher in the Electrical Engineering Department at the Helsinki University of Technology (nowadays part of Aalto University). He finished his Ph.D. thesis in 2005, and at the same time moved to work in the semiconductor industry, where he held both technical and sales roles at Spansion, Altera, and Intel. Since co-founding Xiphera in 2017 Matti has been the full-time Managing Director of Xiphera. More_information **Session Chair:** Professor Lars Dittmann, Technical University of Denmark
10:00-10:30	**Coffee Break & Exhibition**
10:30-12:00 3*30 min	**Presentations** **Session Chair:** Lennart FPGAworld **Title: RISC-V® on Intel® FPGA** **Presenter:** Nikolay Rognlien, Arrow Electronics, Norge **Title: Python and the art of building a high-quality reusable verification environment.** **Presenter:** Faïçal Chtourou, Field Application Engineer, Digital Verification Technologies, Siemens EDA (for InnoFour BV) **Title: Efficient and flexible path to implement hardware/software interfaces** **Presenter:** Bernd Röckert, Eccelerators GmbH, Austria

12:00-13:00	**Lunch Break & Exhibition**
13:00-14:30 2*30 min	**Presentations** **Session Chair:** Lennart FPGAworld **Title: PolarFire® SoC, differentiated application-class embedded processing** **Presenter:** Martin Kellermann, Microchip Ltd, UK **Title: Zero-effort RTL bugs handling** **Presenter:** Dr. Reuven Dobkin, CTO of vSync Circuits, Israel **Title: How to cut development time through automation with CI/CD** **Presenter:** Andrew Swirski, Beetlebox, UK
14:30-15:00	**Coffee Break & Exhibition**
15:00-16:00	**Students Presentations** **Session Chair:** Lennart FPGAworld **Title: A new FPGA-based DSP System for Professional Audio Applications** **Presenters:** Christian Epe and Bernhard M. Riess, University of Applied Sciences Duesseldorf, Germany Article **and** PPT **Title: DeepHLS v.2: Automating high-performance Deep Neural Network implementation on FPGA using High-Level Synthesis** **Presenter:** Mohammad Riazati, Mälardalen University, Sweden
16:00 -	**Go Home Drink in Exhibition Hal**

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Stockholm 12 September and Copenhagen 14 September

More information

Presentations

Title: Efficient and flexible path to implement hardware/software interfaces
Presenter: Bernd Röckert, Eccelerators GmbH, Austria

Abstract:
All designs require communication between HW and SW.
This interface is often already planned in the concept phase and accompanies the project until the final product. Therefore, this point is a very important part of the development. Unfortunately, it often happens that because of project pressure the quality of it suffers. Because what was defined in a concept phase may later turn out to be not ideal or practical. But a change during the project development is often rejected with "too much effort", "what if when something goes wrong" or "then I have to change all other files like documentation or test, too". And exactly here the interface description language HxS helps you. It offers you the possibility to change the registers at any time with maximum flexibility without sacrificing quality.
HxS includes a generator for several output formats such as HDL, SW, test and documentation files. Thus, for each member of the project, the corresponding files are automatically recreated. This also allows everyone work on the same version. Copy and paste errors are also eliminated.
The unique interface description (HxS) also offers the possibility to use different domain structures. With this domain structure you can easily create your own library. Which allows the reuse of existing interfaces and improves the collaboration in the team.
In this presentation I would like to give you an insight into our HxS interface description.
Presenters Bio:
Bernd is one of the four founding members of Eccelerators GmbH. He started his engineering career in the field of FPGA development in 2015 after his successful master's degree at the University of Applied Sciences in Augsburg as an electrical engineer. Since then, he also expanded his FPGA area of expertise there to include the topic of regression testing on real HW, as well as everything related to DevOps itself. During this time, he also continued his education in the area of SW development. In the company Eccelerators he is active in the area of SW development and testing.

Title: Python and the art of building a high-quality reusable verification environment.
Presenter: Faïçal Chtourou
Field Application Engineer, Digital Verifcation Technologies, Siemens EDA (for InnoFour BV)

Abstract:
Constrained randomization and functional coverage have recently become crucial elements to a successful tape out. SystemVerilog and UVM framework is the de-facto standard for verification. Still, due to a high learning time/benefit ratio, many users preferred to look into other alternatives such as UVVM/OSVM.
Lately, Python has emerged as a third option, and it is gaining interest for its obvious advantages (easy language, big community, extensive library …). The purpose of this presentation is to show you how we can build a high-quality reusable verification environment using Python Libraries/Framework.

Title: PolarFire® SoC, differentiated application-class embedded processing
Presenter: Martin Kellermann, Microchip Ltd, UK

Abstract:

Many applications today suffer from constraints on size, power and thermal capabilities. Microchip PolarFire® SoC devices, based on 64-bit quad-core RISC-V application processors, tackle these constraints and allow users to approach and build applications often deemed impossible. The presentation will explain the background on why PolarFire devices solve many of the challenges in such applications as vision or communication-based designs and will show use-cases of designs only made possible by small form factor, low-power FPGAs.

Title: How to cut development time through automation with CI/CD
Presenter: Andrew Swirski, Beetlebox, UK
Abstract:
FPGA development is in a crisis. 68% of FPGA projects were behind schedule in 2020 and only 17% of FPGA projects had no bugs escape into production, according to Wilson Research Group. How can we get projects completed on time and error free even as our chips become larger and more advanced? The answer is automation. In this presentation we will explore how teams can automate their processes through CI/CD (Continuous Integration/ Continuous Delivery) using Beetlebox's new tool BeetleboxCI.

Title: RISC-V® on Intel® FPGA
Presenter: Nikolay Rognlien, Arrow Electronics, Norge

Abstract:
The RISC processor architecture has a long history and since its very beginnings as the "Berkeley RISC" in 1981 it has gone through various architecture generations. In 2010 the first RISC-V® implementation came to live at UC Berkeley and meanwhile this has emerged quite significantly. Today, different variants of 32-/64-/128-bit architectures exist, and the specification continues to be developed. The list of members in the RISC-V® organization is quite long and there are a few silicon devices and development boards available from different sources now.

Intel® who is a Premium Member of the RISC-V® organization does have a RISC type soft processor called NIOS® II which is used in the Intel® FPGAs already for more than a decade. Although Nios® II is highly versatile and configurable, it uses its own proprietary instruction set and tools.

Now Intel® has emerged its soft processor portfolio and started to ship the new FPGA soft processors called Nios® V/m which has a RISC-V® RV32IA compatible architecture. This not only enables much higher performance compared to the Nios® II but also allows to utilize the huge RISC-V® infrastructure and eco-system.

During this session we will look at the architecture and configuration options of the Nios® V/m core compared to the Nios® II processor version. We will investigate the hardware/software development and debugging flows as well as the usable eco-system.

Title: Zero-effort RTL bugs handling
Presenter: Dr. Reuven Dobkin, CTO of vSync Circuits, Israel

Abstract:

RTL bugs are traditionally discovered using dynamic simulation, consuming time, and requiring high effort to achieve a satisfying coverage. During this lecture we will review common bugs that may appear in a few popular RTL implementation approaches for FSMs, reset logic, bus logic, and more. We will show how these bugs can be automatically identified and reported, without running the simulation, thus significantly reducing the verification effort.

Title: A new FPGA-based DSP System for Professional Audio Applications
Presenters: Christian Epe and Bernhard M. Riess, University of Applied Sciences Duesseldorf, Germany

Abstract:
We present a new field-programmable gate array (FPGA) based digital audio signal processing system. Our prototype achieves a performance that up to now has been preserved to costly high-end solutions. Main components of the system are an A/D-converter, an FPGA to perform the digital signal processing, and a D/A-converter. To demonstrate the quality of the audio signal processing, infinite and finite impulse response filters and a delay effect were realized on the FPGA. The measured results are compared to state-of-the-art systems with respect to performance, size, and cost.

Title: DeepHLS v.2: Automating high-performance Deep Neural Network implementation on FPGA using High-Level Synthesis
Presenter: Mohammad Riazati, Company/school/university: Mälardalen University, Sweden

Abstract:
FPGA implementation of Deep Neural Networks is challenging for neural network designers since they usually have limited knowledge of hardware. We propose an automatic toolchain to use High-Level Synthesis (HLS) for this purpose. Firstly, a fully automated tool for creating a synthesizable C implementation from Keras is created. Then, since HLS only transforms a C implementation, and the parallelism capability of a device is not utilized, HLS directives are found through a two-stage design space exploration to create a high-performance implementation with minimal latency.

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